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(54) Input/output control system.

(57) In an input/output control system: a read/write operation for a control register (REG) under a program mode is achieved by hardware; the system, per se, is started or stopped under the control of firmware, and a data transfer in the system is achieved under the control of hardware. Therefore, a high speed data communication is realized, via the system, between a central control unit (CC) and an input/output unit (IO).

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INPUT/OUTPUT CONTROL SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an input/output control system (herein abbreviated as IOC) which performs a transmission control of data communicated between a central control unit (below, abbreviated as CC) and an input/output unit (herein abbreviated as IO). More particularly, it relates to an IOC capable of a high operation speed and having a high reliability.

2. Description of the Related Art

The IOC operates to control an IO, such as a typewriter, magnetic tape apparatus, magnetic disk apparatus, and so on. Recently, IO has come under the control of a microprogram. In general, the processors operated by such a microprogram control are classified into two types: (i) a bit-slice processor, and (ii) a one-chip processor

The bit-slice processor (i) has a high processing speed, in the order of nanoseconds, and a high processing capability, and thus the bit-slice processor is frequently used for a high speed IOC. In the bit-slice processor, however, a special microprogram is necessary, and therefore, the processor has disadvantages in that it is not beneficial from the viewpoint of a general-purpose applicability in firmware, and that it design of relevant hardware and firmware is difficult.

The one-chip processor (ii) does not, however, have the disadvantages inherent to the bit-slice processor (i), and therefore the one-chip processor can be utilized over a wider practical range, compared with the bit-slice processor. The one-chip processor does, however, have a disadvantage in that the processing speed, on the order of nanoseconds, of the one-chip processor is lower than that of the bit-slice processor. The IOC to which the present invention is adapted is controlled with the one-chip processor.

The prior art IOC has two major features, as explained hereinafter. First, a direct memory access (so called DMA) transfer is realized by a microprogram, and second, an interruption to a microprocessor (μP) takes place every time a program mode (PM) operation is initiated during a DMA transfer.

In view of the above-mentioned two features, two problems arise in prior art IOC. First, a data transmission rate is lowered, and accordingly, a high speed IOC cannot be expected, and second, the related firmware is very complicated. Note, an example of such prior art IOC is shown in U.S. Patent No. 4,467,454.

SUMMARY OF THE INVENTION

Accordingly, an object of the present invention is to provide an IOC having a higher operation speed and simpler firmware relative to the aforementioned prior art IOC.

To attain the above object, in the IOC which is connected, via a common bus (C-BUS), with a central control unit (CC), and further connected, via an external-bus (E-BUS), with an I/O so that the IOC performs a transfer of data to be communicated between the CC and the I/O, the system (IOC) is featured by employing, first, a buffer memory for momentarily storing therein the transfer data and reading the same therefrom, second, a control register for writing therein data transfer control information sent from the CC, and third, a direct memory access control means for reading the data transfer control information from the control register and then achieving, by means of the buffer memory, the data transfer control, and the data transfer is carried out by accessing an address specifying a desired I/O, wherein the overall data transfer in the IOC is controlled by a microprocessor mounted therein, which executes a microprogram to start and stop the data transfer.

BRIEF DESCRIPTION OF THE DRAWINGS

The above object and features of the present invention will be more apparent from the following description of the preferred embodiments with reference to the accompanying drawings, wherein:

Fig. 1 illustrates a typical and conventional input/output control system, mounting therein a one-chip microprocessor, and adjacent members thereof;

Fig. 2 shows a register structure forming the program mode control register (PMREG);

Fig. 3 is a circuit diagram illustrating a principle construction of an input/output control system according to the present invention;

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Before describing the embodiments of the present invention, the related art and the disadvantages therein will be described with reference to the related figures.

Figure 1 illustrates a typical and conventional input/output control system, mounting therein a one-chip microprocessor, and adjacent members thereof. In Fig. 1, IOC represents an input/output control system. The IOC is connected, via a common bus C-BUS, with a central control unit CC, and is also connected, via an external bus E-BUS, with an input/output unit IO.

A variety of IO's exist in a computer system; herein a magnetic disk unit (DKU) is illustrated as an example, but the input/output unit IO may be a typewriter, a cathode ray tube (CRT) display, and the like.

A nucleus of the IOC is the one-chip microprocessor μP which, via an internal bus I-BUS, receives data from a read only memory (ROM) and a random access memory (RAM), and via the I-BUS, also sends data to the RAM. Further, the μP is connected via gates GT1 and GT3 being, for example, open-collector type gates, with a program mode control register PMREG and a direct memory access mode data register DMAREG, respectively. These two registers PMREG and DMAREG are further connected with the common bus C-BUS, via gates GT2 and GT4, respectively. Furthermore, the microprocessor μP is connected with a direct memory access mode control circuit - (DMACTL) and an interruption control circuit - (INTCTL). These circuits DMACTL and INTCTL, a program mode control circuit (PMCTL), and an input/output address matching circuit (IOAM) are connected with the common bus C-BUS. The other buses, I-BUS and E-BUS, are interconnected via an input/output unit control circuit IOCTL.

It should be understood that the central control unit CC is usually connected, via the common bus C-BUS, with a plurality of IOC's, however, in Fig. I, only one IOC, connected with the magnetic disk unit DKU, is representatively displayed. The members in each IOC play the following rolls.

(a) The input/output address matching circuit IOAM determines whether or not the data, transferred on the common bus C-BUS, has an address which specifies the own side IOC, so that the circuit IOAM can selectively recognize an own side IOC form among a plurality of IOC's.

(b)The program mode control circuit PMCTL performs a data transfer under a program mode executed by the central control unit CC.

(c)The program mode control register PMREG acts as a buffer for a data transfer under the program mode.

(d)The direct memory access mode data register DMAREG acts as a buffer for a data transfer under the DMA mode.

(e)The direct memory access mode control circuit DMACTL achieves a data transfer under the DMA mode.

(f)The interruption control circuit INTCTL controls the interruption operation.

(g) The input/output unit control circuit IOCTL controls the input/output unit IO.

The above-mentioned functional members operate as follows. In this explanation of the operations, a content of a control register will be first related, which control register stores program control words. The program control words, in the example, are loaded in the random access memory RAM.

Figure 2 shows a register structure forming the program mode control register (PMREG). It should be understood here that the program control words are transferred, via the register PMREG, to the control register formed in the RAM. As seen from Fig. 2, the program control words are set up with a device status register (DSR), a file address register (FAR), a command resister (CMR), a memory address register (MAR), and a word count register - (WCR), each being composed of 16 bits. These registers are allotted respective addresses, for example, 200 through 204. The address are particularly defined on the common bus C-BUS and applied to respective IOC's connecting with the C-BUS.

The above-mentioned registers play the following roles.

(a) The device status register DSR acts as a flag area for indicating a status of the own side IOC. For example, the statuses "data is now being transferred", "data transfer is finished" and so on, are indicated in the flag area.

(b) The file address register FAR indicates a file address specifying a desired file data

central control unit CC. Also, the microprogram sets an interruption information in the area, corresponding to the device status register DSR, in the memory RAM. Thus, a series of operations in the IOC system is finished and the IOC system is left as it is until a next start is effected thereto.

As understood from the above, the typical and conventional IOC suffers from two problems. First, a direct memory access (DMA) transfer is realized by the use of the microprogram, and therefore, a data transmission rate is lowered and a high speed IOC cannot be expected, and second, an interruption to the microprocessor takes place every time the program mode (PM) is activated, and therefore, the construction of the related firmware becomes complicated.

To overcome the above mentioned problems, a person skilled in the art may first conceive of employing a data transfer between the circuit IOCTL and the memory RAM performed under the DMA mode. This concept, however, is not advantageous, since the rate of data transfer between the memory RAM and the common bus C-BUS does not become high, but is left as it is, so that the operation speed of the IOC system is not improved as a whole.

Figure 3 is a circuit diagram illustrating a principle of the construction of an input/output control system according to the present invention. In Fig. 3, members identical to those of previous figures are represented by the same reference characters (as for all later figures). Therefore, compared with Fig. 1, a major difference in construction, lies in the employment by the IOC system of Fig. 3 of a buffer memory. In the example of the present invention, the buffer memory is comprised of a first-in/first-out (FIFO) memory. For this, a selector (SEL) and an input/output unit direct memory access control circuit (IDMACTL), other than the circuit DMACTL, are introduced thereto. Further, a diagnostic check portion (DIGC) is introduced to the IOC system of the present invention. The DIGC portion is not an indispensable constituent for the present invention, but is beneficial to the present invention. That is, the DIGC carries out a desired diagnostic check operation in cooperation with, under control of the microprocessor μP and/or the central control unit CC, the circuit IDMACTL, the circuit DMACTL and the buffer memory (FIFO).

The buffer memory, e.g., the memory FIFO, momentarily stores the transfer data to be communicated between the common bus C-BUS and the input/output unit control circuit IOCTL. The selector SEL, cooperating with the memory FIFO, selects either a transfer data from the internal bus I-BUS or a transfer data from the common bus C-BUS. The input/output unit direct memory access control circuit IDMACTL, cooperating with the memory FIFO, achieves a control of a data transfer between the input/output unit control circuit IOCTL and the memory FIFO.

In the IOC system, of the present invention, both a write operation and a read operation, under the program mode (PM), with respect to a control register REG in the system IOC, are achieved by the use of hardware. When a command information is written in the command register CMR, which sends commands for various operations to the system IOC, an interruption is made to the microprocessor μP and then a microprogram is started for activation of the IOC system. When a data transfer series comes to end, that is the operation of the IOC system is ended, an interruption is made from the circuit IOCTL to the microprocessor μP to start the microprogram for stopping the data transfer.

The operation of the IOC system is summarized as follows. The DMA transfer of the transfer data, communicated between the IO and the central control unit CC, is achieved without using a microprogram, as in the typical and conventional IOC system. In place of this microprogram, the transfer data traffic is regulated by the memory FIFO. Accordingly, the microprogram is used only for, first, when the IOC system is to be started, starting the input/output unit IO in accordance with the contents of the control register REG, and second, when the operation of the system IOC comes to an end, for editing an interruption information to be applied to the central control unit CC to execute an interruption command. In conclusion, the IOC system according to the present invention incorporates as many as possible automatic hardware operations, and thus a high speed IOC system can be realized.

The benefits obtained by an employment of the diagnostic check portion DIGC, will be summarized below. As mentioned above, the data transfer is mainly performed with the use of hardware, represented by the memory FIFO, and thus a portion sandwiched between the unit CC and the unit IO (DKU) becomes seemingly empty. Therefore, once a problem occurs during the data transfer, a relatively long time is needed to carry out troubleshooting. That is, it is difficult to rapidly determine whether the problem has occurred in the memory FIFO, the unit IO or the microprocessor μP. This causes an apparent deterioration in the reliability of the IOC system. To counter this, the diagnostic check portion is introduced thereto, to ensure reliability in the IOC system. The functions of the diagnostic check part are largely classified

tion which will be explained in detail hereinafter.

12 Direct memory access mode control circuit (DMACTL)

The circuit DMACTL achieves a transfer control of data, under a DMA mode, to be transferred between the common bus C-BUS and the FIFO memory. The circuit DMACTL is also an indispensable member for realizing the diagnostic check operation which will be explained in detail hereinafter.

13 Selector (SEL)

The selector SEL functions as a selection circuit for inputting, to the FIFO memory, either data from the internal bus I-BUS or data from the common bus C-BUS, selectively. The selector SEL is related to the diagnostic check described later.

14 Internal bus (I-BUS)

The bus I-BUS is mounted in the processor system having the microprocessor μP at a center portion thereof. That is, the bus I-BUS functions as a microprocessor bus. The bus I-BUS is also related to the diagnostic check described later.

(B) Explanation of address map (Fig. 5)

An address allocation, viewed from the microprocessor μP, in the IOC system, is referred to as an address map.

Figure 5 shows an example of an address map defined in the IOC system.

1 The addresses 0 through 0FFF, in terms of hexadecimal notation, are allotted to the random access memory RAM.

2 The addresses 1000 through 1004 are allotted to the control register REG, which operates to buffer the program control words and so on for controlling the IOC system. More specifically, the address 1000 is allotted to the device status register DSR, 1001 to the file address register FAR, 1002 to the command register CMR, 1003 to the memory address register MAR, and 1004 to the word count register WCR.

Note, the addresses allotted to the above mentioned registers DSR, FAR, CMR ... are not the same as those shown in previous Fig. 2 by 200, 201, 202 .... This is because, the addresses 200, 201, 202 ... are not addresses viewed from the microprocessor μP, but are defined particularly on the common bus C-BUS, as mentioned previously.

3 In this example, the addresses 1005 through 3FFF are not used.

4 The address 4000 is used for indicating the status of the FIFO memory. The status of the FIFO memory is expressed as "FULL" or "EMPTY". The former status indicates that the FIFO memory is full of transfer data, and the latter status indicates that all of the transfer data has been output from the FIFO memory and no transfer data remains therein.

Note, the above mentioned two statuses can be detected as respective electric signals, output from terminals FUL and EMP provided by the FIFO memory, as shown in Fig. 4.

5 The address 4001 is an area used for indicating an interruption command to be issued to the common bus C-BUS.

6 The address 4002 is allotted to the control register, mounted in the input/output unit control circuit IOCTL, which buffers control information for controlling the input/output unit IO.

7 In the example, the area with curved hatchings after the address 4003 is not used.

8 The address 8000 is an area used for specifying a write or read operation with respect to the FIFO memory. The address 8000 is effective during the diagnostic check operation by the DIGC.

9 The address 8001 is allotted to the information "DIR", "IDMAEX", and "DMAEX". The information DIR (abbreviation of direction) is used for specifying a direction in which the transfer data TD is to be transferred. The information "IDMAEX" and "DMAEX" are effective during the diagnostic check operation by the DIGC, and are used, respectively, for exciting the input/output unit direct memory access control circuit ID-

CMR, the transfer direction specifying bit DIR (refer to the address 8001 in Fig. 5) is determined, and then the flip-flop DIR•F/F - (Fig. 4) is set or reset in conformity with the bit information DIR. At this time, the input/output unit control circuit IOCTL (Figs. 3 and 4) is started. Further, the circuit IOCTL, after starting the input/output unit IO, controls this unit IO to prepare for the data transfer (refer to step "b" in Fig. 6A). Thereafter, the microprogram waits for the occurrence of a next interruption (refer to "INTERRUPTION WAIT" in Fig. 6A). During the "WAIT INTERRUPTION", a diagnostic check is performed inside the IOC system, if necessary.

In the above recited step "a" of Fig. 6A, if the content of the command register CMR loaded in the memory RAM indicates a "read operation", the output logic of the flip-flop DIR•F/F is set as "0" (refer to "0": READ in Fig. 4). In this case, if the status of the FIFO memory is not "FULL", that is, there are empty areas in the FIFO memory, the input/output unit direct memory access control circuit IDMACTL is started to draw data, read from the unit DKU, from the input/output unit control circuit. The thus-obtained data is set in the FIFO memory. Meanwhile, the FIFO memory is placed to a FULL status, so that the activation of the control circuit IDMACTL is released.

When the FIFO memory is not placed to an EMPTY status, that is, data remains in the FIFO memory, the data must be sent to the common bus C-BUS. Each time this data send occurs the content of the memory address register MAR is automatically incremented by +1, to renew the write address for the main memory MM to the next write address. Also, the content of the register FAR is incremented by +1, but the content of the register WCR is decremented by -1. As mentioned above, the data read from the unit DKU is automatically transferred and output to the common bus C-BUS.

In the above recited step "a" of Fig. 6A, if the content of the command register CMR loaded in the RAM indicates A "write operation", the output logic of the transfer direction specifying flip-flop DIR•F/F is set as "1" (refer to "1": WRITE in Fig. 4). In the write operation, as in the above mentioned read operation, the data transfer is smoothly performed through the FIFO memory. At the same time, the registers MAR and FAR are incremented by +1, respectively, while the register WCR is decremented by -1, each time a data transfer is completed. The related incremental and decremental counts are carried out automatically by hardware.

4 Figure 6B is a flow chart for exhibiting a series of operations generated by an interruption for finish issued from the input/output unit control circuit (IOCTL). When a transfer of a predetermined amount of data is finished, the circuit IOCTL issues an inter ruption for finish to the microprocessor μP. At this stage, some transfer data may not yet have been transferred, and remains in the memory FIFO. Therefore, after confirmation that the FIFO memory is in the EMPTY status, an interruption is issued to the interruption control circuit INTCTL, whereby a series of data transfers is completed.

In step "c" of Fig. 6B, it is determined whether the finish of the control circuit IOCTL is normal (YES) or not (NO). When the finish is normal, step "d" follows thereafter. In step "d", it is determined whether the status of the FIFO memory is EMPTY or FULL. If the memory FIFO is in the EMPTY status, step "e" follows thereafter.

In step "e", a normal interruption status is set in the device status register DSR.

Thereafter, in step "f", a command for an interruption is issued to the interruption control circuit INTCTL.

In step "c", if it is determined that the finish is not normal or an error occurs in the common bus C-BUS, the operation is brought to an end at step "g". In step "g", an abnormal interruption status is set in the device status register DSR. In this case, the interruption for finish operation may be carried out not immediately by an interruption request, but by a resultant condition after a plurality of activations of the circuit IOCTL.

5 Figure 6C shows the step generated when a common bus (C-BUS) error occurs. Step "h" of Fig. 6C is led to step "g" of Fig. 6B via symbols ". If the some problem occurs on the common bus C-BUS side, the related

tion, commanded by the circuit IDMACTL, is commenced when certain conditions are satisfied. First, the transfer direction specifying flip-flop DIR•F/F - (corresponding to DIR at address 8001 in Fig. 5) is set as logic "0", i.e. READ. The logic "0" from the DIR•F/F is applied to a gate G1 at one inputs thereof, and accordingly, if the logic "0" is also applied to the other input thereof, the gate G1 is opened. (Note: each small circle, i.e., o, denotes logical inversion, as for all later figures). Therefore, the gate G1 is opened if the FIFO memory is in a non-FULL status, where the related input of the gate GI is connected via a line L4 to the terminal FUL of the FIFO memory.

When the gate G1 is opened, the input/output unit direct memory access control circuit is started, via a gate G3 which is an OR gate, so that a signal RD, i.e., read command, is issued therefrom and the circuit IOCTL is instructed, by the signal RD, to operate under a read mode (R). Then the read operation of date from the unit DKU commences. A signal WT indicates a command for write, which is applied to the circuit IOCTL at an input W thereof, which represents a write mode.

The thus read date from the magnetic disk unit DKU is supplied to the FIFO memory, via the line L3 and the selector SEL. The input terminal S1 of the SEL is made conductive under the condition where the write operation is not specified. An input terminal S3 of the SEL is led, via a line L5, to the circuit IDMACTL at a supply terminal thereof of a signal WT', i.e., a write command. In this case, the FIFO memory must be operated under the write mode (W). This condition is satisfied by the reception of the command signal WT' for a write operation, which is given to the FIFO memory at the write mode specifying terminal W, thereof, via a gate G5, i.e., an OR gate.

If the FIFO memory is not in the FULL status, the read data stored in the FIFO memory is output from an output terminal D_{out} thereof to the common bus C-BUS. During the output of the read data to the common bus C-BUS, first the FIFO memory must be operated under the read mode (R). The read mode (R) is set by first starting the circuit DMACTL and then applying a command signal RD for a read, operation, sent from the circuit DMACTL, to the FIFO memory, at a read specifying terminal R thereof, via a line L7 and the gate G4.

In the above case, the condition wherein the control circuit DMACTL is started is that in which three inputs of a gate G6, i.e., an AND gate, are all supplied with logic "0", except for an input thereof led to the flip-flop DIR•F/F. The latter input is now supplied with the logic "0", since the read operation is now conducted. Due to the thus opened gate G6, the output from the gate G6 starts the control circuit DMACTL via a gate G9, i.e., an OR gate. Accordingly, a transfer of the stored data commences from the FIFO memory to the common bus C-BUS.

The above-mentioned three inputs of the gate G6, except for the input led to the DIR•F/F, are supplied with three kinds of signals, respectively. First is a time out signal given from a time supervisor (TIMSV) via a line L9, which indicates a time out occurring on the common bus C-BUS. Second is a signal indicative of EMPTY given, via a line L10, from the terminal EMP of the FIFO memory. Third is a signal indicative of "WCR = 0" given from the register WCR in the control register REG - (Fig. 3). With the reception of these signals, the gate G6 is opened, which signals represent that, first a time out has not occurred on the common bus C-BUS, second, the FIFO memory is not in the EMPTY status, and third the word count number - (WCR) is not zero. The above mentioned common bus time out specifically means a time out of a control signal S_{CTL} given to the common bus C-BUS side. To be specific, the time out occurs in a case such that, although the control circuit DMACTL issued a request in the form of the signal S_{CTL} for outputting the stored data in the FIFO memory to the common bus C-BUS, a response thereto is not made from the central control unit CC, even though a predetermined time has elapsed.

The content of the memory address register MAR is incremented by +1 under control of the circuit DMACTL, each time stored data is read out from the FIFO memory. On the other hand, the content of the word count register WCR is sequentially decremented by -1. When the content of the register WCR reaches zero, the control circuit DMACTL stops sending data to the common bus C-BUS. This is common to both the write operation and read operation, and therefore, the signal indicative of "WCR = 0" is supplied to not only the gate G6 but also a gate G7, i.e., an AND gate. In this case, information indicating the EMPTY status of the FIFO memory, other than the above information indicative of "WCR = 0", is also necessary to release the activation of the control circuit DMACTL.

Similarly, in a write operation, a value corresponding to an amount of data to be transferred is preset in the register WCR. Therefore, the content of the register WCR does not reach zero at that time, a write request for the unit DKU is sequentially issued from the input/output system IOC side, i.e., a master side under the DMA mode, to the central control unit CC side, i.e., a slave side

Figure 8A illustrates a schematic general view for explaining the diagnostic check with respect to the FIFO memory. That is, Fig. 8A shows a diagnostic mode for the FIFO memory. Under the diagnostic mode, the aforesaid commands for data transfer, performed with the FIFO memory, are stopped. These commands are issued from the control circuits DMACTL and IDMACTL. Note, the circuits DMACTL and IDMACTL are not illustrated in Fig. 8A. Thus, both the units CC and IO are cut off from the FIFO memory.

Next, a predetermined diagnostic check data DD is written, via a route I, in the FIFO memory, under control of a microprogram, by the microprocessor μP. The data DD can be stored in advance in the ROM (Fig. 3). The thus written data DD is then read therefrom and sent to the microprocessor μP, via a route II. If no problem exists in the FIFO memory, the data DD is correctly returned to the microprocessor μP.

Figure 8B illustrates a schematic general view for explaining the diagnostic check with respect to both the memory FIFO and the unit IO. That is, Fig. 8B shows a diagnostic mode for both the FIFO and the IO. Under the diagnostic mode, the circuit DMACTL stops issuing the aforesaid command for data transfer to the FIFO memory, and thus only the circuit IDMACTL operates as usual. Note, only the circuit IDMACTL is illustrated in Fig. 8B. Thus, first the central control unit CC is cut off from both the FIFO memory and the input/output unit IO.

Next, under control of a microprogram by the microprocessor μP, a predetermined diagnostic check data DD is written, via a route I, in the FIFO memory read again from the FIFO memory, and is written in the input/output unit IO via a route II. The thus written data DD in the unit IO is read via a route III, written in the FIFO memory, and read again therefrom to be again sent to the microprocessor μP via a route IV. If no problems exist in both the FIFO memory and the unit IO, the data DD is correctly returned to the microprocessor μP. If the data DD is not correctly returned, it is determined that a malfunction exists in the FIFO memory and/or the unit IO, and an alarm is issued from the microprocessor μP to warn of the occurrence of a malfunction.

In the above mentioned case, a further investigation must be made to determine whether the problem has occurred in the FIFO memory or in the unit IO. If the FIFO memory is normal, it is judged that the problem exists in the IO unit. Conversely, if the FIFO memory is abnormal, it is possible that the malfunction exists in both the FIFO memory and the IO unit. In this case, it is necessary to first repair the FIFO memory and then determined whether or not the IO unit is abnormal. Note, the diagnostic mode for the FIFO memory, mentioned previously in reference to Fig. 8A, can be utilized for the investigation into whether the FIFO memory is normal or abnormal.

Figure 8C illustrates a schematic general view for explaining the diagnostic check with respect to both the FIFO memory and the common bus C-BUS. That is, Fig. 8C shows a diagnostic mode for both the FIFO memory and the C-BUS. Under the diagnostic mode, the circuit IDMCTL stops issuing the aforesaid command for data transfer to the FIFO memory, and thus only the circuit DMACTL operates as usual. Note, only the circuit DMACTL is illustrated in Fig. 8C. Thus, first the input/output unit IO is cut off from both the FIFO memory and the central control unit CC.

Next, under control of the microprogram by the central control unit CC, a predetermined diagnostic check data DD is written, via a route I, in the FIFO memory, read again from the FIFO memory, and fetched by the microprocessor μP via a route II. The data fetched by the microprocessor μP is read and written from and to the FIFO memory again via a route III. The thus written data is read out again by the central control unit CC via a route IV. If no problem exists in either the FIFO memory or the common bus C-BUS, the data DD is correctly returned to the central control unit CC. If the data is not correctly returned thereto, it is determined that a problem exists in the FIFO memory and/or the common bus C-BUS. Thereby, an alarm is issued from the central control unit CC to warn of the occurrence of the problem.

In the above mentioned case, a further investigation must be made into whether the problem has occurred in the FIFO memory or in the common bus C-BUS. If the FIFO memory is normal, it is judged that the problem exists in the common bus C-BUS. Inversely, if the FIFO memory is abnormal, it is possible that the problem exists in both the FIFO memory and the common bus C-BUS. In this case, it is necessary to first repair the FIFO memory and then investigate whether or not the common bus C-BUS is abnormal. Note, the diagnostic mode for the FIFO memory, mentioned previously in reference to Fig. 8A, can be utilized for the investigation into whether the FIFO memory is normal or abnormal.

Figure 9 illustrates a schematic general view for explaining a data processing mode by the microprocessor μP. In the data processing mode, the transfer data TD provided from the central control unit CC is processed by the microprocessor μP, and the thus processed data is written, as a processed data td, in the IO unit. Under the pro-

The read operation from the FIFO memory is achieved every time a read command "READ" is issued from the microprocessor μP and set in the register REG (Fig. 5) at the address 8000 thereof. To be specific, among the gates G30 through G35 (refer to left side of Fig. 10), each being an AND gate, the gate G35 is opened. (When the write command "WRITE" is issued, the gate 30 is opened.). Then the output from the gate G35 passes through a gate G42 (corresponding to the gate G4 of Fig. 4), among the gates G40 through G42 each being an OR gate, so that the memory FIFO is operated under the read mode (R). At this time, a gate G50 (illustrated at right bottom side of FIFO memory) is also necessarily opened to make a gate G51, i.e., a transfer gate, active, and thereby a transfer route led to the internal bus I-BUS, is made conductive. On the other hand, a transfer route, led to the external bus E-BUS, is made conductive by a gate G52, i.e., a transfer gate, which is made active by the information for the excitation of IDMAEX. Note, during the read operation under the usual DMA transfer mode, both gates G33 and G34 are opened, respectively, by a read request IDMARD and a read request DMARD. These requests IDMARD and DMARD (corresponding to signals RD' and RD shown in Fig. 4) are given from the control circuits IDMACTL and DMACTL, respectively. Therefore, these gates G33 and G34, together with the gate G42, comprise the gate G4 shown in Fig. 4.

The operation to write to the first-in/first/out memory FIFO is achieved every time a write command "WRITE" is issued from the microprocessor μP and set in the register REG (Fig. 5) at the address 8000 thereof. The write command bit is applied to a gate G60 (AND gate) and activates a gate G61 (transfer gate) to make a transfer route from the I-BUS conductive. While a transfer route, let to the external bus E-BUS, is made conductive by a gate G62, i.e., a transfer gate, which is made active by the information for the excitation of IDMAEX. Note, during the write operation under the usual DMA transfer mode, both gates G31 and G32 are opened, respectively, by a write request IDMAWT and a write request DMAWT. These requests IDMAWT and DMAWT (corresponding to signals WT' and WT shown in Fig. 4) are given from the control circuits IDMACTL and DMACTL, respectively. Therefore, these gates G351 and G352, together with the gate G41, comprise the gate G5 shown in Fig. 4.

Throughout the descriptions mentioned above, it is believed that the spirit and basic concept of the present invention can be sufficiently comprehended by person skilled in the art. Supplemental explanations, however, will be given below in order to further clarify the IOC system according to the present invention, by dislosing detailed examples thereof.

Figures 11A and 11B depict timing charts for explaining an information transfer carried out on the common bus C-BUS. As seen from these figures, the information transfer is carried out between a master device M and a slave device S at any time. The transfer is commanded from the master device M at any time, and where the central control unit CC acts as the master device M, is known as a program mode (PM) transfer, and where the IOC system acts as the slave device S, it is known as a direct memory access (DMA) mode transfer.

When a device, provided by the bus C-BUS, acts as the master device M, it is necessary to execute a sequence for acquiring a bus activation right. This is not particularly pertinent, and therefore, no further explanation will be given.

The information transfer from the master device M (hereinafter simply master M) to the slave device S (hereinafter simply slave S), i.e., M → S, is executed as follows.

(1) The master M issues a signal BBSY having a logic "1", which signal indicates, to other devices, that the bus is now being activated, i.e., a bus busy signal.

(2) The master M issues, to address bits 2^0 through 2^{15}, an address of the control register REG in the IOC system, under the PM, and an address of a memory inside the CC, under the DMA. At the same time, a parity of data is issued on a parity line PTY.

(3) The master M issues information to data bits 2^0 through 2^{15}.

(4) The master M makes a signal WSRVI logic "1", so that the slave S is informed that the information is supplied to the C-BUS; this signal is the so called write service in signal.

(5) When the slave S detects that the logic of the signal WSRV is "1", it receives the data and stores the same at a portion specified by the address bits. This portion is the register REG under the PM, and is the DMA memory under the DMA. At the same time, the slave S makes a line SRVO to be logic "1"; this line is the so called service out line.

operation has finished abnormally; the conditions CEH = "1" and CEL = "0" denote that the operation has finished normally, and the conditions CEH = "1" and CEL = "1" denote that the command is invalid. In Fig. 13B, the bits ICMD are used to set an IOCTL command therein.

Figure 14 is a partial perspective view of the magnetic disk unit (DKU). Fig. 14 is referenced for an explanation of the following table.

Table

COMMAND	OPERATION	COMMAND (hexadecimal notation)	COMMAND PARAMETER
READ DATA	DATA PART OF SPECIFIED SECTOR IS READ AND SENT TO HOST.	BO	CN HN SN SCNT
WRITE DATA	DATA FROM HOST IS WRITTEN IN SPECIFIED SECTOR.	FO	CN HN SN SCNT

The above table displays an example of commands and command parameters. In the table, CN denotes a cylinder number, HN a head number, SN a sector number, and SCNT a number of the sectors.

Figure 15 illustrates a common bus connection area of Fig. 4 in more detail. The common bus C-BUS is mainly composed of an address line, a data line, and a control line. Note, members relating to the program mode (PM) are omitted, since Fig. 15 displays members pertinent to the present invention. The DMA transfer between the bus C-BUS and the memory FIFO is started by the signal WREQ2 or RREQ2 (Fig.10) given from the peripheral of the FIFO memory. When the circuit DMACTL is started by the above mentioned signal, the information transfer, explained in reference to Figs. 11A and 11B, commences execution. A detailed explanation of the operation concerned will be given hereinafter.

Figure 16 illustrates peripherals of the FIFO memory. It should be understood that the peripherals of Fig. 16 is arranged to be adopted to the control registers, relating to the FIFO memory, allotted to the addresses 4000, 4001 and 4003 of the address map shown in Fig. 12. The write/read allocation at the address 4001 is achieved through the microprocessor (μP) bus, illustrated as "BUS" in Fig. 16. On the other hand, the write/read allocation at the address 4003 is achieved through the internal bus I-BUS of Fig. 16.

In Fig. 16, the signals "WRITE" and "READ" represent instructions for write and read issued from the microprocessor μP. The address signals indicative of 4000, 4001, and 4003 are formed by decoding the addresses given from the microprocessor μP. Signals DMAWT and DMARD represent instructions for write and read given from the control circuit DMACTL. Signals IDMAWT and IDMARD represent instructions for write and read given from the control circuit IDMACTL. The transfer request signals, i.e., WREQ1, WREQ2, RREQ1, and RREQ2, are selectively generated in accordance with the internal status of the FIFO memory and the content of the control register at the address 4001.

Figure 17 illustrates peripherals of the circuit IOCTL. It should be understood that the peripherals of Fig. 17 are arranged to be adopted to the control register, relating to the circuit IOCTL, allotted to the addresses 4004 and 4005 of the address map shown in Fig. 12. The write/read allocations at the addresses 4004 and 4005 are achieved through the bus I-BUS connected, via a bidirectional driver, to the bus BUS.

Accordingly, the C-BUS time out detection time is defined with the time up to the overflow of the counter. The operation of the circuit shown in Fig. 24 will be further clarified with reference to Fig. 25.

Figure 25 depicts timing charts for clarifying the operation of the time supervisor (TIMSV) illustrated in Fig. 24. In Fig. 25, the triangle symbol at the bottom thereof represents the time at which the time out concerned is detected. Further, the dotted lines represent the case where the C-BUS operation is performed normally.

Figure 26 illustrates a detailed example of the input/output control circuit (IOCTL). It should be understood that the IOCTL of Fig. 26 is set up for, among a variety of input/output units, the magnetic disk unit DKU. Therefore, the unit DKU is controlled by the IOCTL by way of a usual DKU interface control circuit, which is not pertinent to the present invention, and therefore, no further explanation will be given therefor. The members shown in this figure are already mentioned in reference to the previous figures. For example, "STR", "ICMR" and "DFIFO" are shown in Fig. 12, and the "READ", "WRITE", "INT", "DREQ" "IOCWT", and "IOCRD" are shown in Fig. 17.

As mentioned above in detail, in the present invention, although the IOC system is operated under a low cost one-chip microprocessor which is easy to use but has a low in operation speed, the IOC system can substantially act as a high speed operation system due to the use of the hardware concerned. In this case, it becomes difficult, in general, to establish a satisfactory diagnostic check due to employment of such hardware. This problem, however, can be overcome with the use of the diagnostic check portion and thus, a prompt restoration from a malfunction state is assured. This attributes to the realization of a highly reliable IOC system.

Claims

1. An input/output control system (IOC), the IOC system being operatively connected, via a common bus (C-BUS), with a central control unit (CC) and being operatively connected, via an external bus - (E-BUS), with an input/output unit (IO), so as to control a transfer of data to be communicated between the central control unit (CC) and the input/output unit (IO) characterized in that

the following three units are further introduced to the IOC system:

a buffer memory in which transfer data is momentarily stored;

a control register (REG) in which a plurality of sets of data transfer control information, given from the central control unit (CC), are written, and;

a direct memory access control means being operative, under a command from a microprocessor - (μP) with the use of data transfer control information written in said control register (REG), to achieve a data transfer control with respect to said buffer memory,

where a data transfer is performed by accessing the input/output unit (IO) via an input/output unit control circuit (IOCTL) for controlling the unit (IO), and both processes for starting and finishing operations of the control circuit (IOCTL) are carried out by the microprocessor (μP) which executes a predetermined microprogram.

2. A system as set forth in claim 1, wherein said direct memory access control means is comprised of an input/output unit direct memory access control circuit (IDMACTL) and a direct memory access control circuit (DMACTL), in which the control circuit (IDMACTL) is operative to perform the data transfer between said buffer memory and the input/output unit control circuit (IOCTL), while the control circuit (IDMACTL) is operative to perform the data transfer between the buffer memory and a common bus (C-BUS) located between the IOC system and the central control unit (CC).

3. A system as set forth in claim 2, wherein a program mode control circuit (PMCTL) is connected with the common bus (C-BUS) to achieve the transfer control under a program mode (PM), and the microprocessor (μP) is directly activated, via the control circuit (PMCTL), by an interruption for activation which occurs when a data transfer request is issued from the central control circuit - (CC) and, when the related data transfer comes to an end, said activation is released by an interruption for finish which is issued from the input/output unit control circuit (IOCTL).

4. A system as set forth in claim 3, wherein said buffer memory is made of a first-in/first-out memory (FIFO).

5. A system as set forth in claim 4, wherein the first-in/first-out memory (FIFO) is provided with an input terminal(D_{in}) for a write data, an output terminal (D_{out}) for a read data, a write mode command reception terminal (W), a read mode com-

15. A system as set forth in claim 14, wherein the diagnostic check part is operative to momentarily stop issuance of said data transfer request to the input/output unit direct access mode control circuit (IDMACTL) and/or the direct memory access mode circuit (DMACTL), selectively.

16. The system as set forth in claim 15, wherein the diagnostic check part (DIGC) is further operative to issue a command for write or read to the first-in/first-out memory (FIFO) under control of said microprogram.

17. The system as set forth in claim 16, wherein the diagnostic check part (DIGC) sets up, at least, a first diagnostic mode, a second diagnostic mode and a third diagnostic mode, selectively, in which, under the first diagnostic mode, a related diagnostic check data (DD) is communicated only between the microprocessor (μP) and the first-in/first-out memory (FIFO), under the second mode, a related diagnostic check data (DD) is communicated only by way of the microprocessor (μP), the memory (FIFO) and the input/output unit (IO), and under the third mode, a related diagnostic check data (DD) is communicated only by way of the microprocessor (μP), the memory (FIFO) and the central control unit (CC).

18. A system as set forth in claim 17, wherein the diagnostic check portion (DIGC) is comprised of logic gates (G20 through G23) at least, the logic gates (G20 through G23) are supplied with at least four sets of information, first, a transfer direction specifying information (DIR) generated by said microprogram, second, an information (IDMAEX) indicative of command for exciting the input/output unit direct memory access mode control circuit (IDMACTL), third, an information (DMAEX) indicative of command for exciting the direct memory access mode control circuit (DMACTL), and fourth, either said "FULL" status information or said "EMPTY" status information regarding the first-in/first-out memory (FIFO), and thus, a read request (RREQ1) given to the control circuit (IDMCTL), a read request (RREQ2) given to the control circuit (DMACTL), a write request (WREQ1) given to the control circuit (IDMCTL) and a write request (WREQ2) given to the control circuit (DMACTL) are output from respective logic gates G20 through G23.

19. A system as set forth in claim 18, wherein the diagnostic check portion (DIGC) is operative to detect that no problem has occurred in the first-in/first-out memory (FIFO), in the input/output unit (IO) and in the microprocessor (μP), respectively under said first, second and third diagnostic modes.

20. A system as set forth in claim 17, wherein the diagnostic check portion (DIGC) is also operative to set up a fifth mode in which the transfer data in the first-in/first-out memory (FIFO) is processed to form another transfer data with the aid of the microprocessor (μP) and then rewritten in the memory (FIFO), so that the thus processed data is stored in the input/output unit (IO).

21. A system as set forth in claim 20, wherein the microprocessor (μP) executes a process for a cipher with respect to said transfer data.

Fig. 3

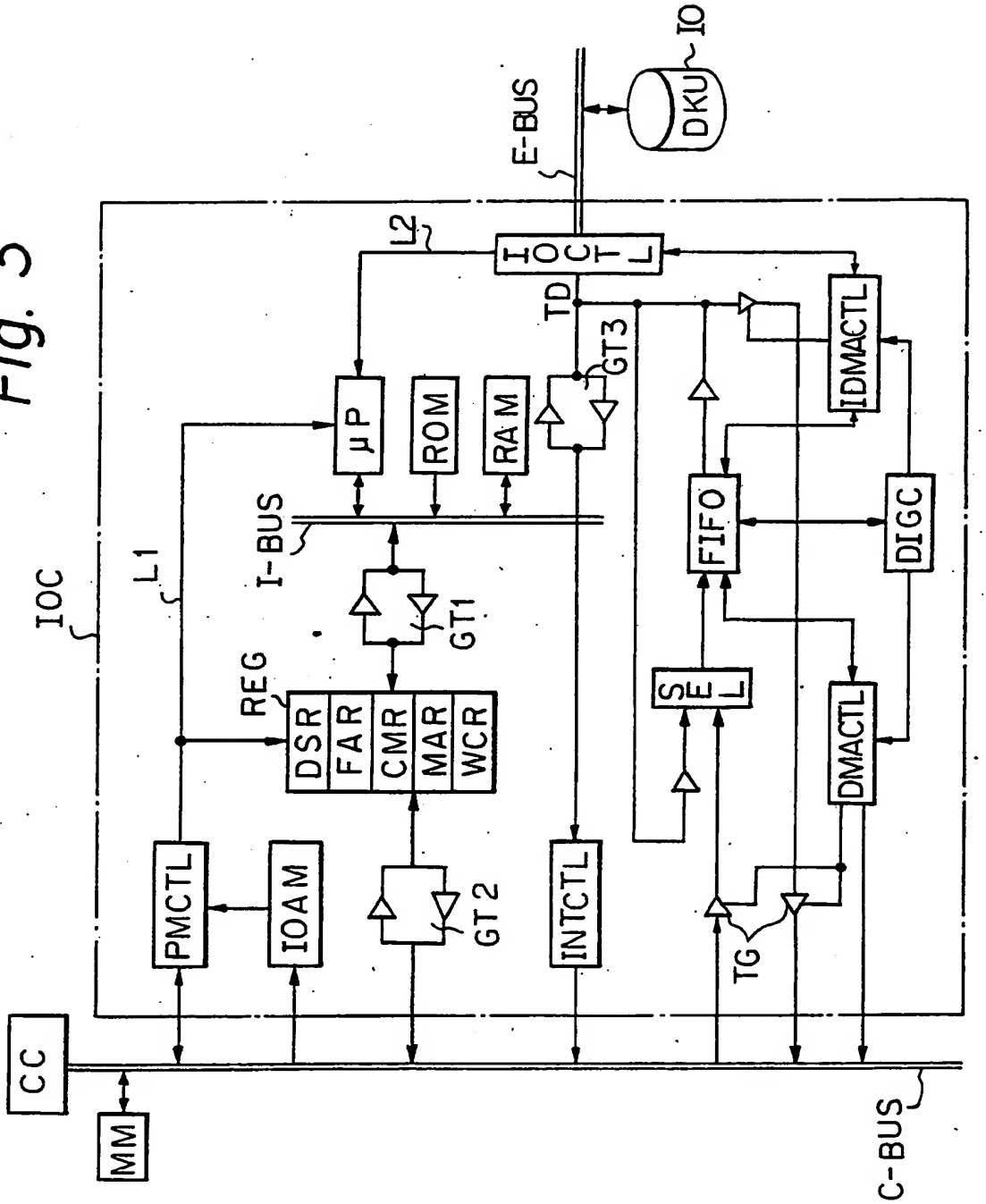

IO
DKU
E-BUS
L2
IOCTL
TD
GT3
IDMACTL
μP
ROM
RAM
FIFO
DIGC
IOC
L1
I-BUS
GT1
REG
DSR
FAR
CMR
MAR
WCR
SEL
DMACTL
PMCTL
IOAM
GT2
INTCTL
TG
CC
MM
C-BUS

Fig. 5

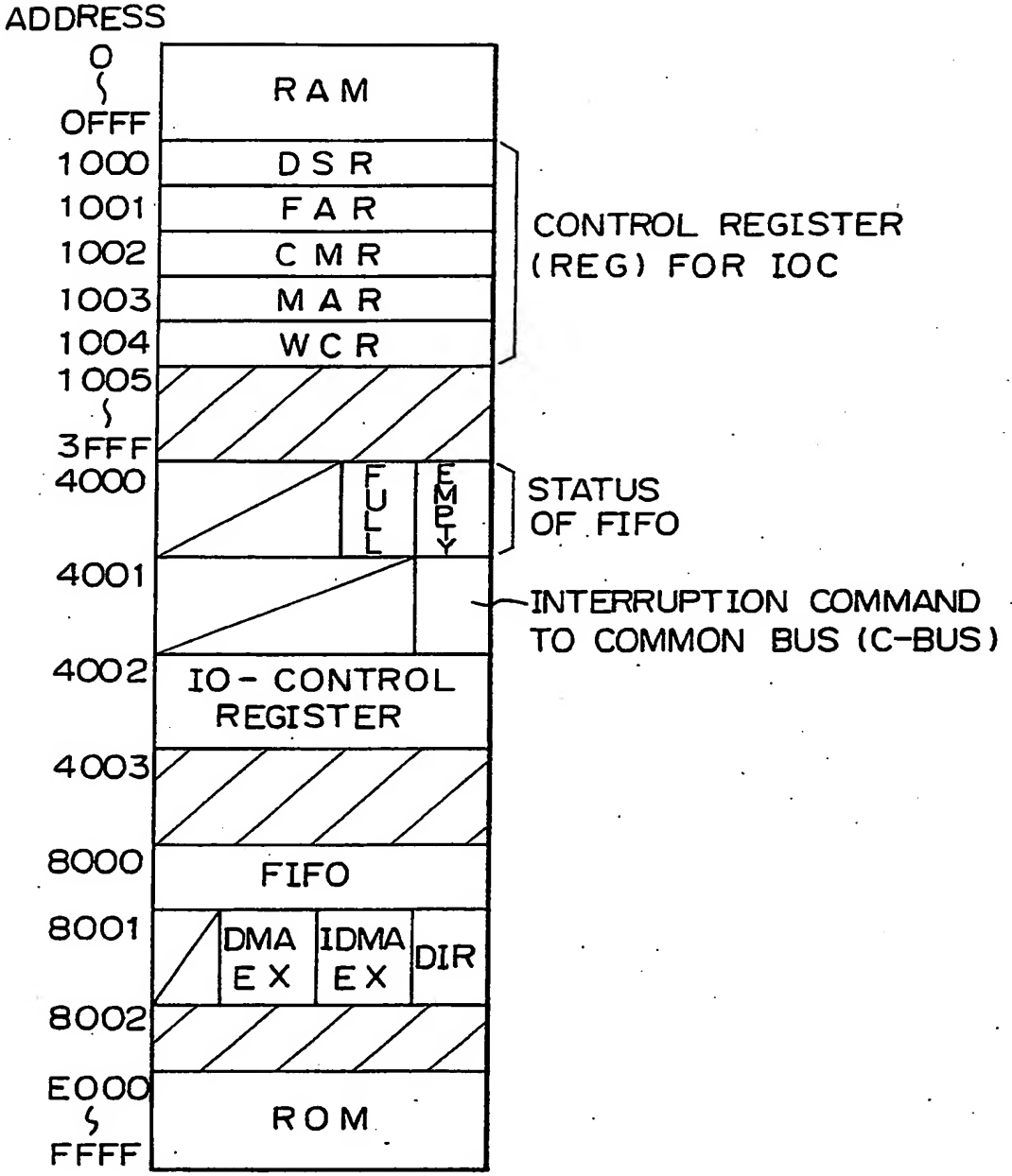

ADDRESS
0
OFFF
RAM
1000
DSR
1001
FAR
1002
CMR
1003
MAR
1004
WCR
CONTROL REGISTER (REG) FOR IOC
1005
3FFF
4000
FULL
EMPTY
STATUS OF FIFO
4001
INTERRUPTION COMMAND TO COMMON BUS (C-BUS)
4002
IO-CONTROL REGISTER
4003
8000
FIFO
8001
DMA EX
IDMA EX
DIR
8002
E000
FFFF
ROM

Fig. 6B

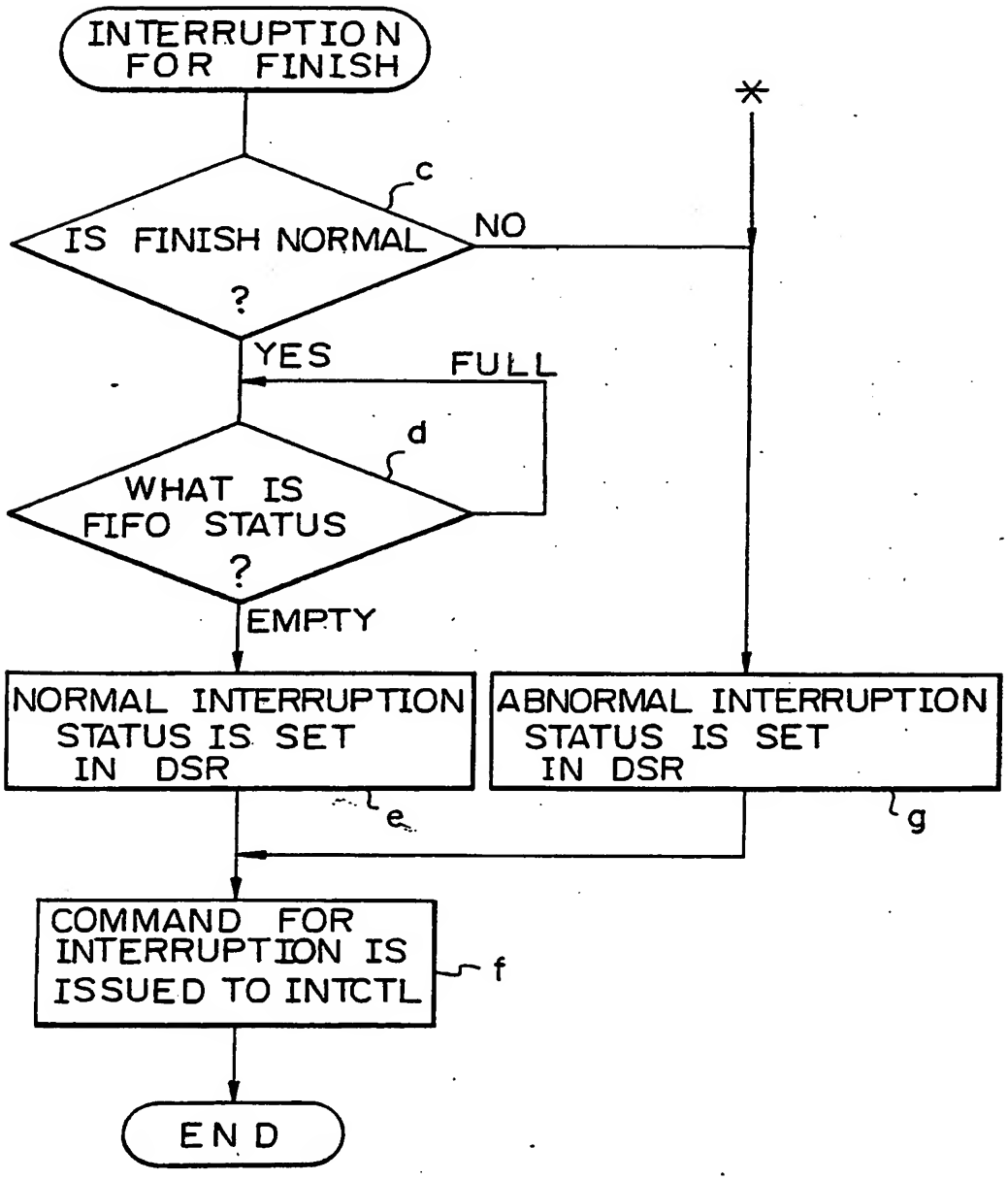
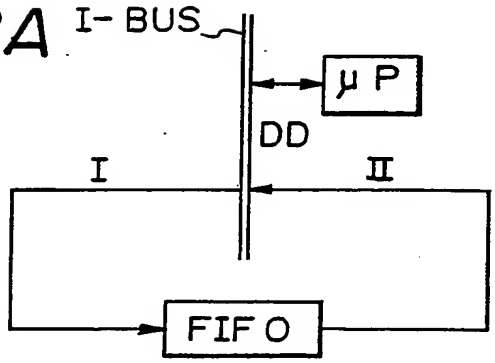

INTERRUPTION FOR FINISH
c
IS FINISH NORMAL ?
NO
YES
FULL
d
WHAT IS FIFO STATUS ?
EMPTY
NORMAL INTERRUPTION STATUS IS SET IN DSR
e
ABNORMAL INTERRUPTION STATUS IS SET IN DSR
g
COMMAND FOR INTERRUPTION IS ISSUED TO INTCTL
f
END

Fig. 8A



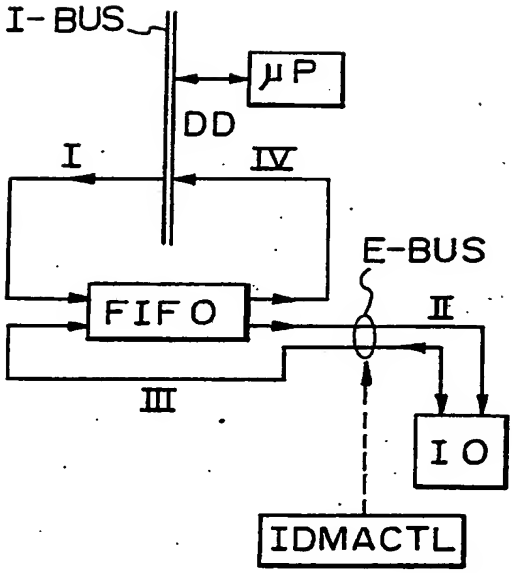


Fig. 8B

Fig. 8C

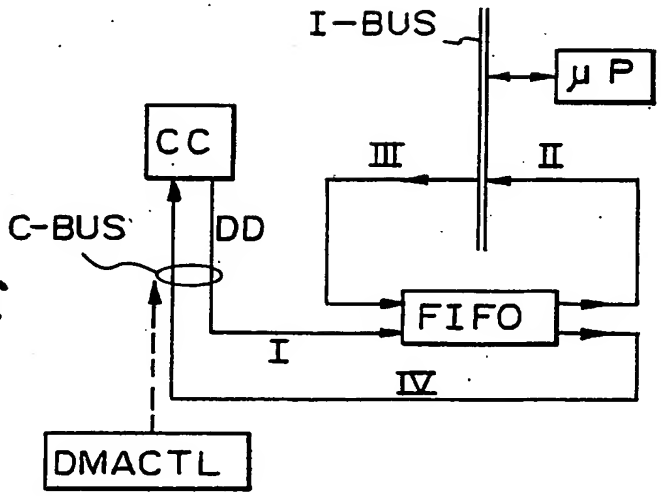


Fig.10

Fig.10A
Fig.10B

Fig. 10A

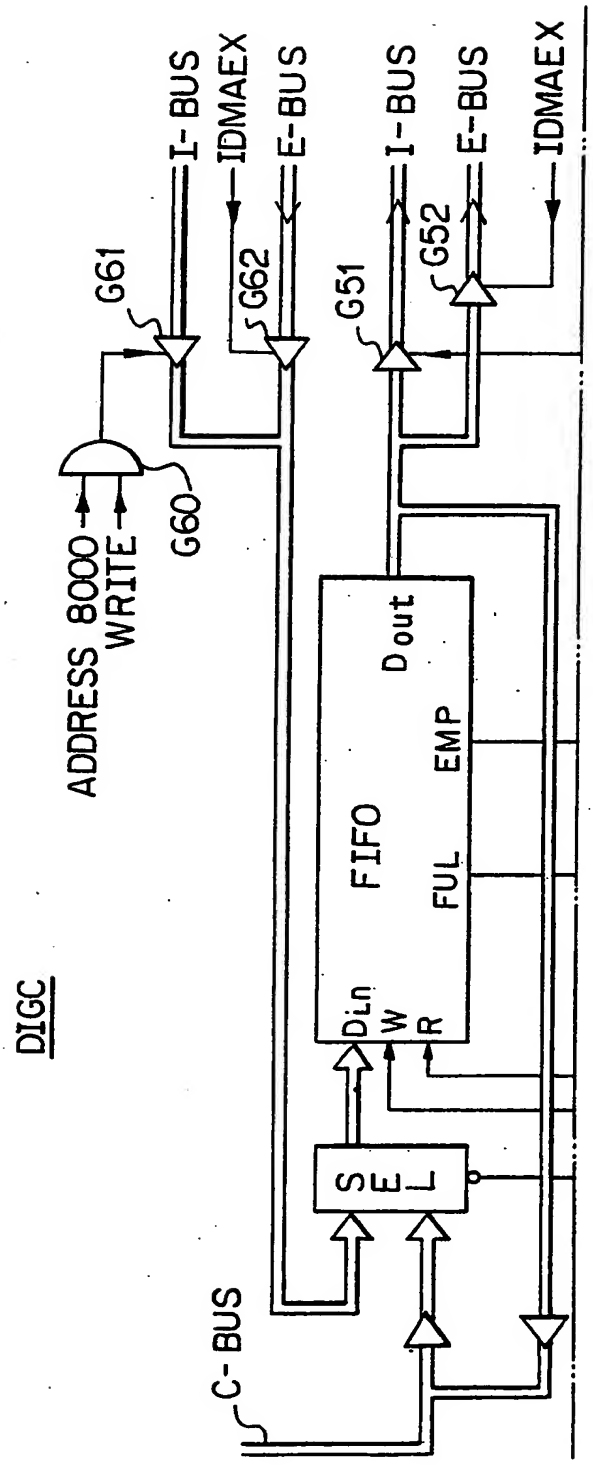


Fig. 11A

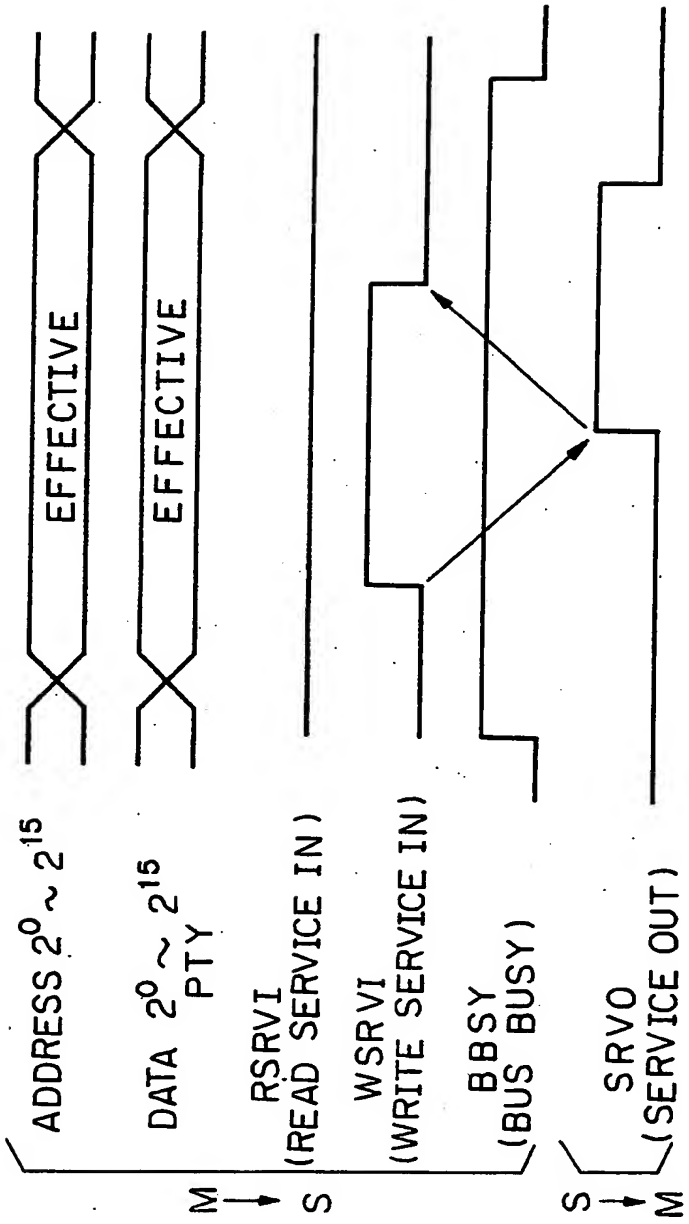

EFFECTIVE
EFFECTIVE
ADDRESS $2^0 \sim 2^{15}$
DATA $2^0 \sim 2^{15}$ PTY
RSRVI (READ SERVICE IN)
WSRVI (WRITE SERVICE IN)
BBSY (BUS BUSY)
SRVO (SERVICE OUT)
M → S
S → M

Fig. 12

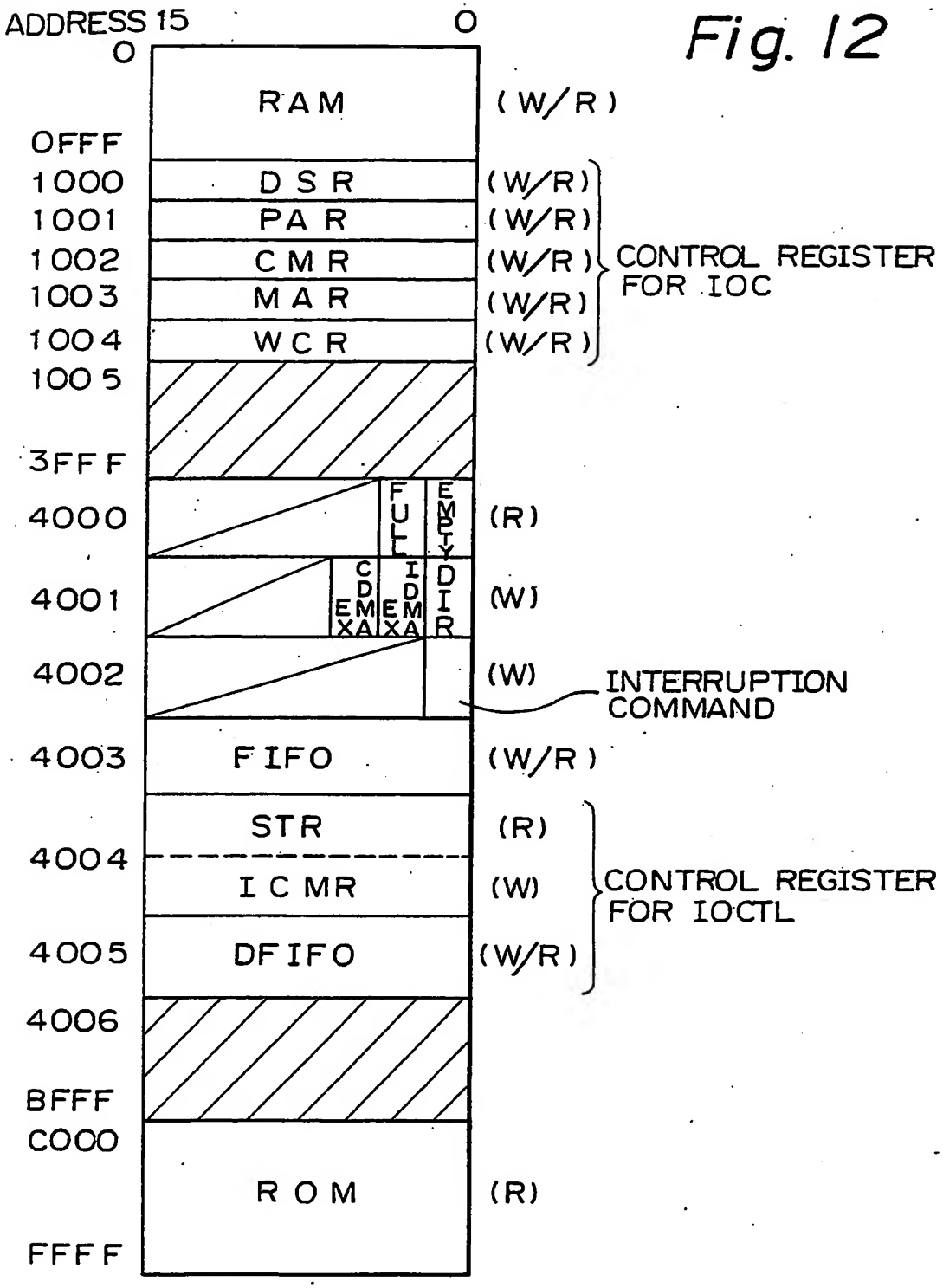

ADDRESS 15
0
0
RAM
(W/R)
0FFF
1000
DSR
(W/R)
1001
PAR
(W/R)
1002
CMR
(W/R)
1003
MAR
(W/R)
1004
WCR
(W/R)
CONTROL REGISTER FOR IOC
1005
3FFF
4000
FULL
EMPTY
(R)
4001
CDMEXA
IDMEXA
DIR
(W)
4002
(W)
INTERRUPTION COMMAND
4003
FIFO
(W/R)
STR
(R)
4004
ICMR
(W)
CONTROL REGISTER FOR IOCTL
4005
DFIFO
(W/R)
4006
BFFF
C000
ROM
(R)
FFFF

Fig. 15

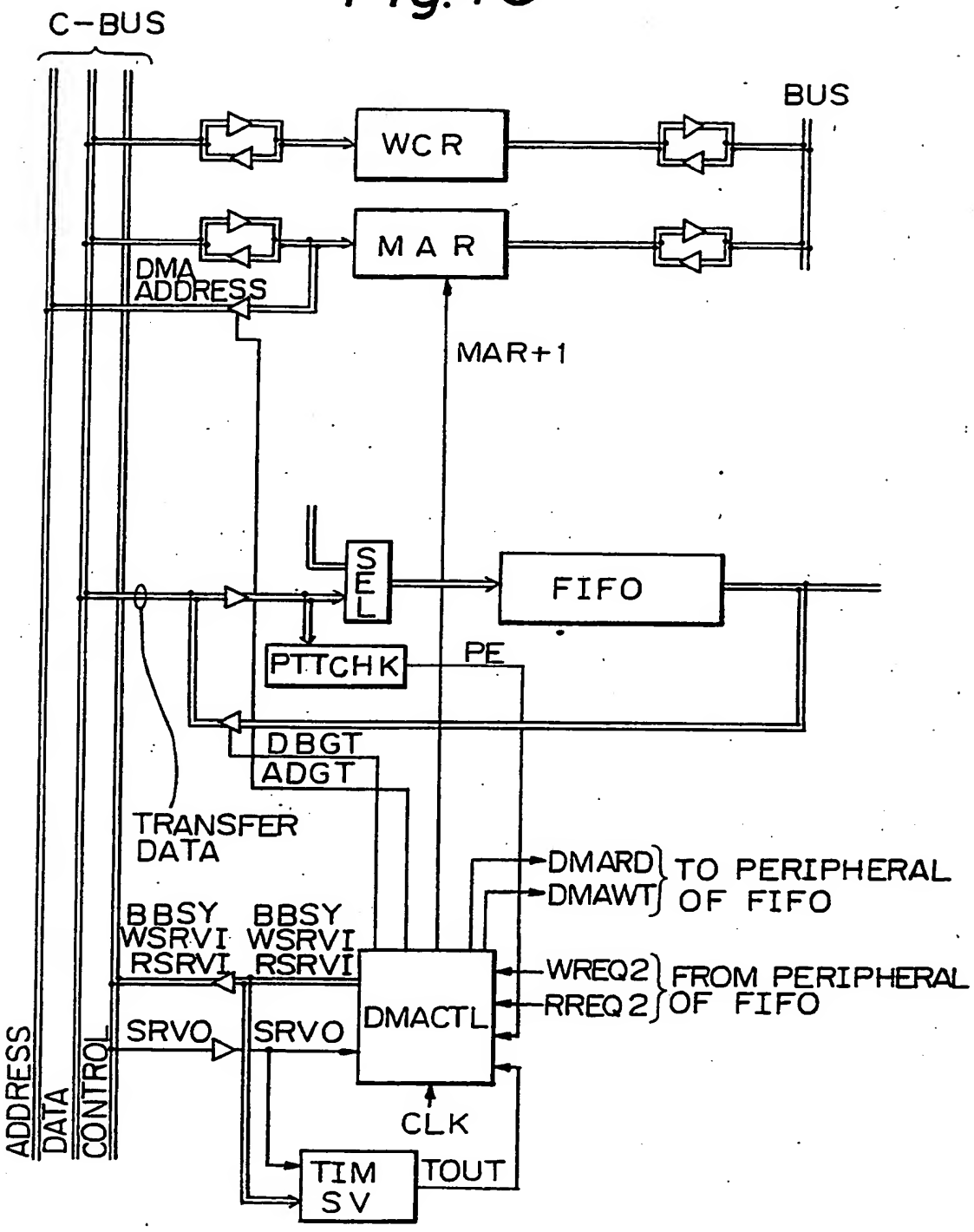

C-BUS
BUS
WCR
MAR
DMA ADDRESS
MAR+1
SEL
FIFO
PTTCHK
PE
DBGT
ADGT
TRANSFER DATA
DMARD
DMAWT
TO PERIPHERAL OF FIFO
BBSY WSRVI RSRVI
BBSY WSRVI RSRVI
WREQ2
RREQ2
FROM PERIPHERAL OF FIFO
SRVO
SRVO
DMACTL
CLK
TIM SV
TOUT
ADDRESS
DATA
CONTROL

Fig. 16B

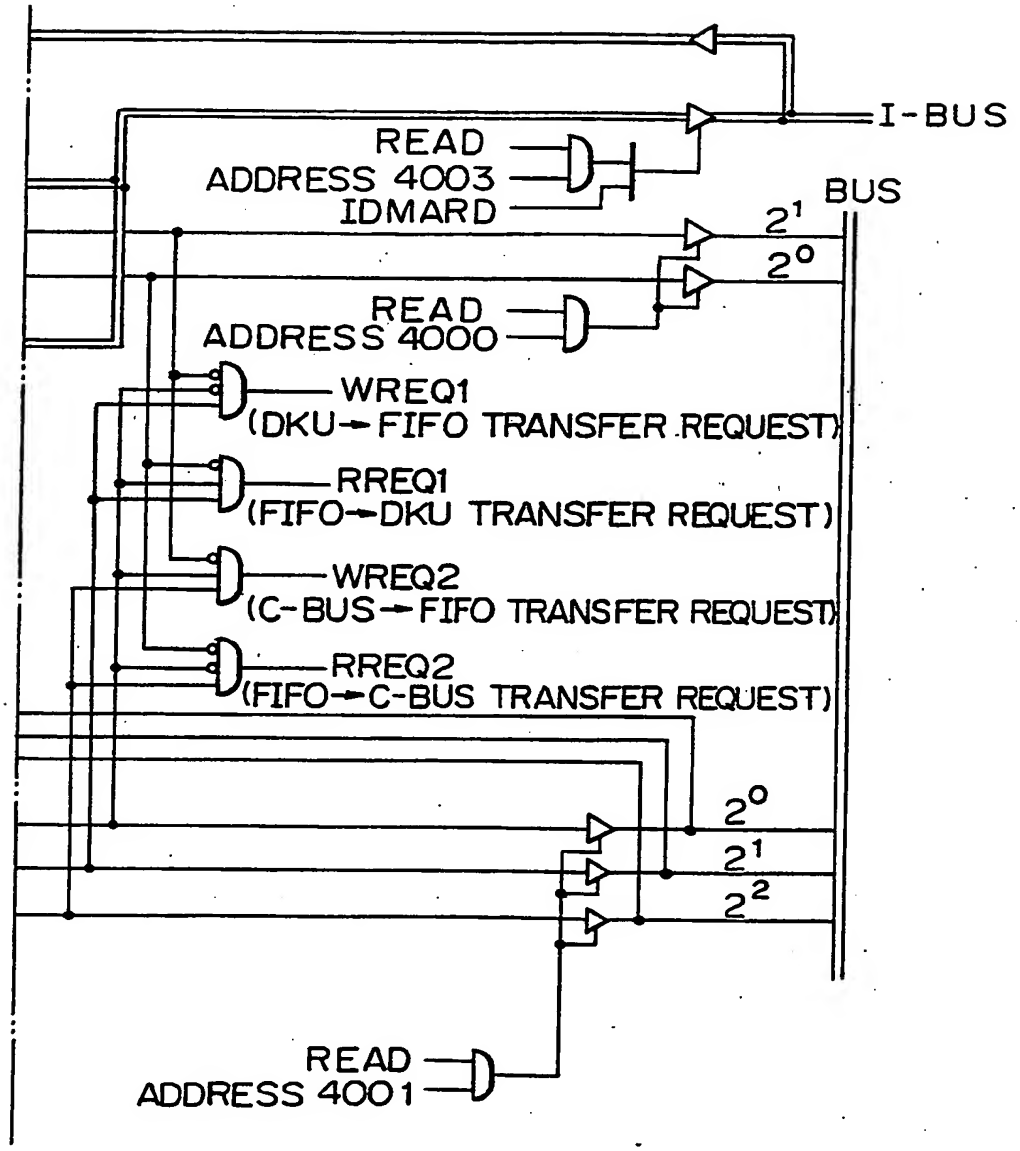

I-BUS
READ
ADDRESS 4003
IDMARD
BUS
2¹
2⁰
READ
ADDRESS 4000
WREQ1
(DKU→FIFO TRANSFER REQUEST)
RREQ1
(FIFO→DKU TRANSFER REQUEST)
WREQ2
(C-BUS→FIFO TRANSFER REQUEST)
RREQ2
(FIFO→C-BUS TRANSFER REQUEST)
2⁰
2¹
2²
READ
ADDRESS 4001

Fig. 18

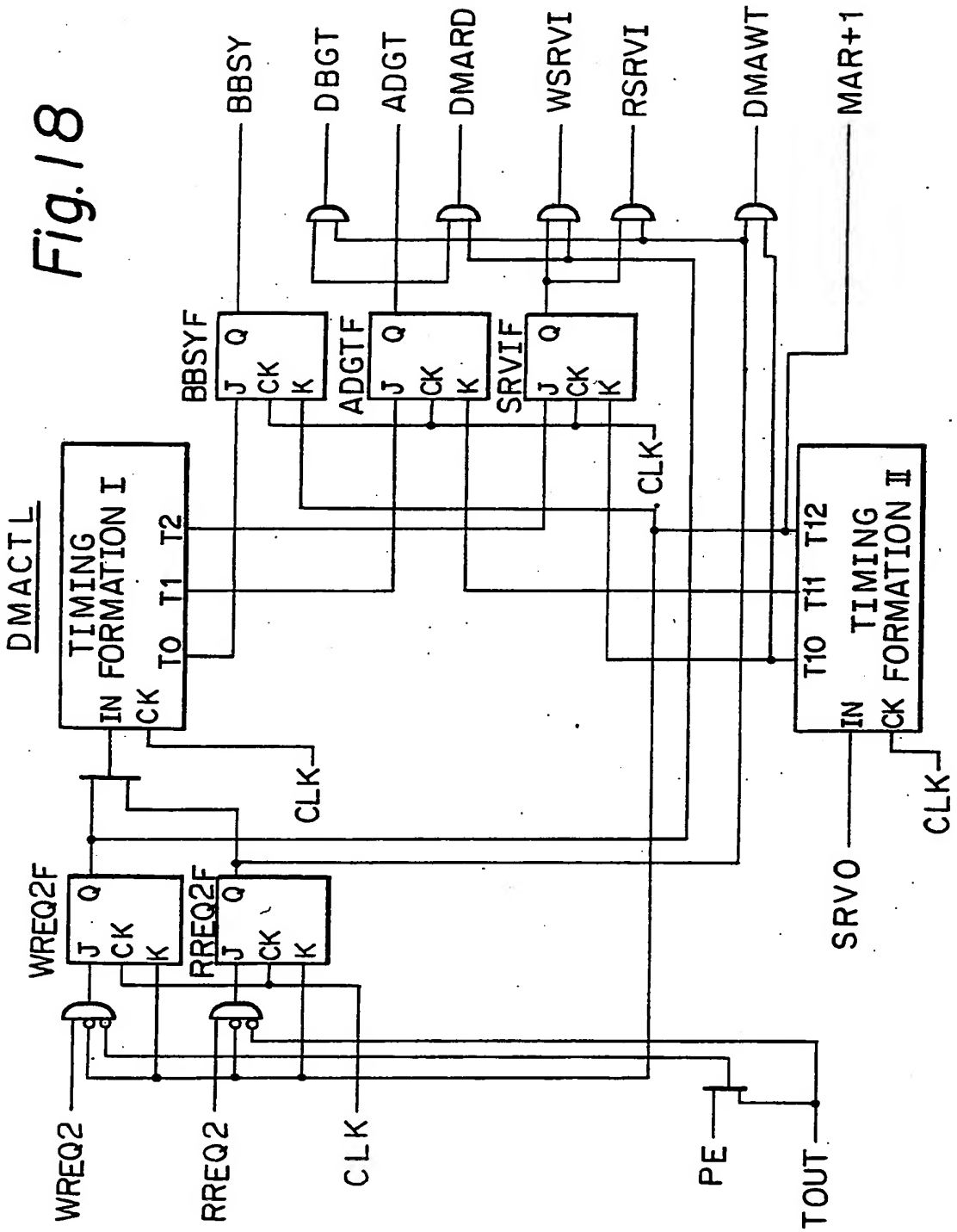

DMACTL
TIMING
IN FORMATION I
CK
T0 T1 T2
BBSY
DBGT
ADGT
DMARD
WSRVI
RSRVI
DMAWT
MAR+1
BBSYF
ADGTF
SRVIF
J Q
CK
K
CLK
TIMING
FORMATION II
IN
CK
T10 T11 T12
SRVO
WREQ2F
RREQ2F
WREQ2
RREQ2
PE
TOUT

Fig. 20

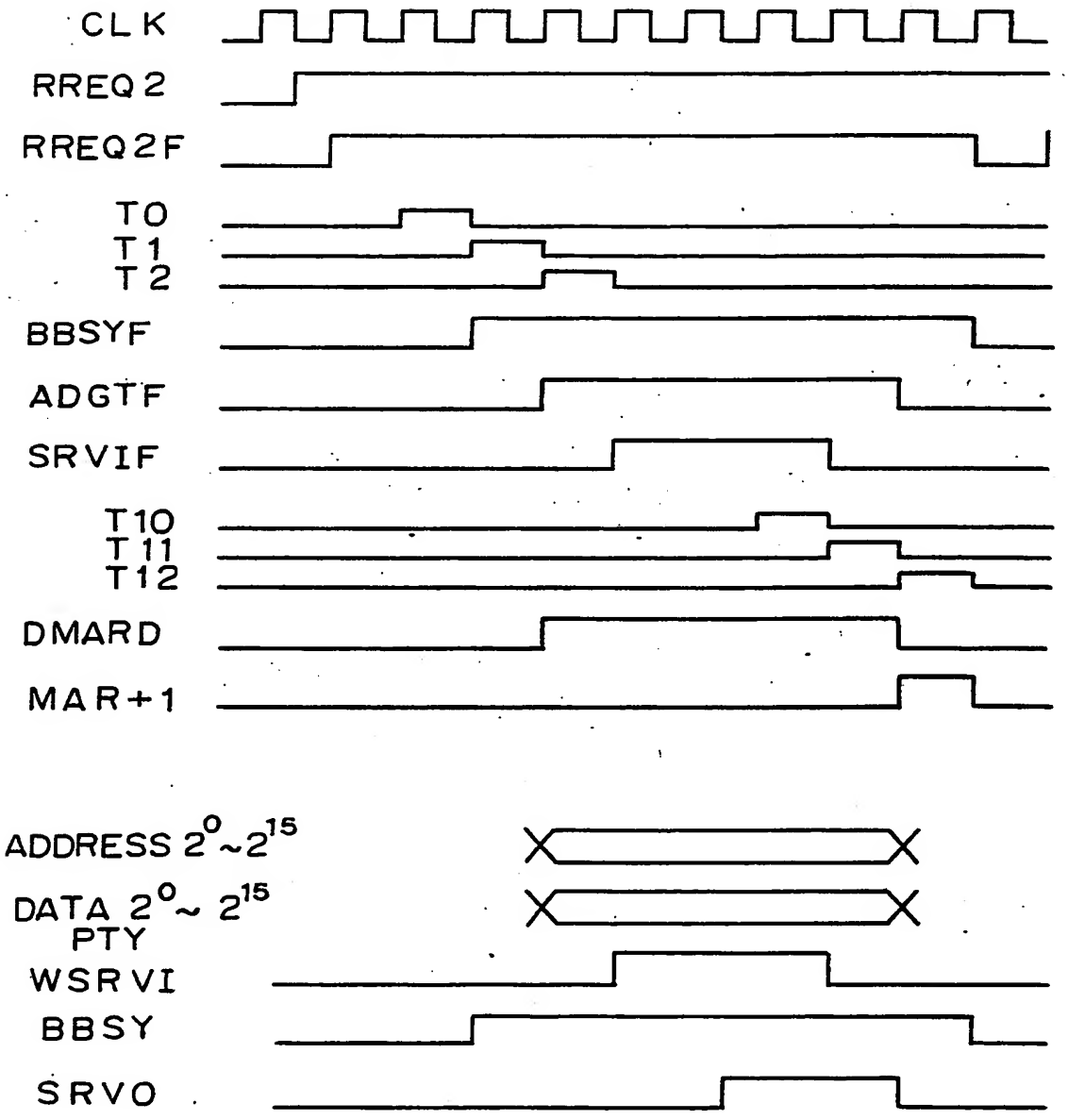

CLK
RREQ2
RREQ2F
T0
T1
T2
BBSYF
ADGTF
SRVIF
T10
T11
T12
DMARD
MAR+1
ADDRESS 2^0~2^{15}
DATA 2^0~ 2^{15}
PTY
WSRVI
BBSY
SRVO

Fig. 23

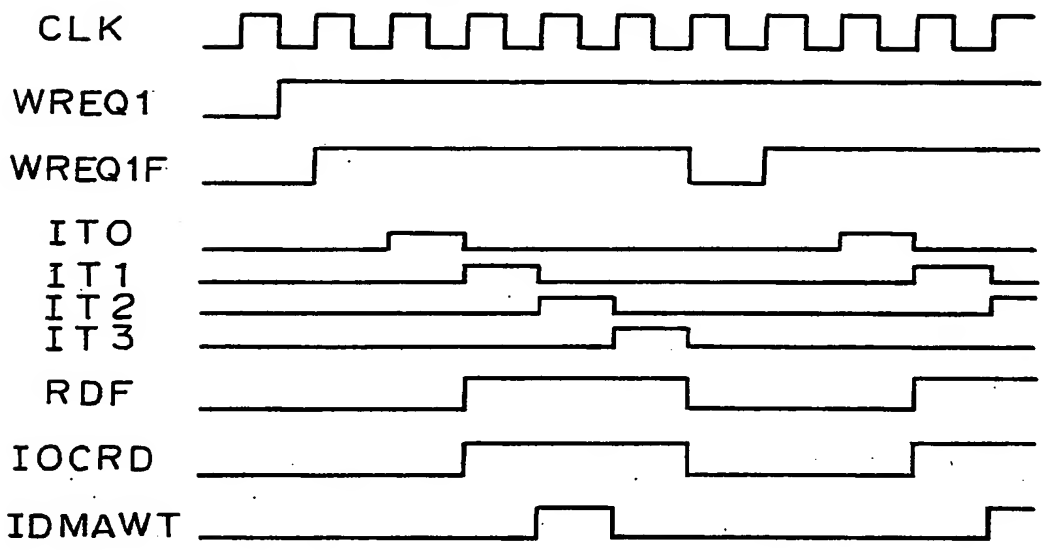

CLK
WREQ1
WREQ1F
ITO
IT1
IT2
IT3
RDF
IOCRD
IDMAWT

Fig. 25

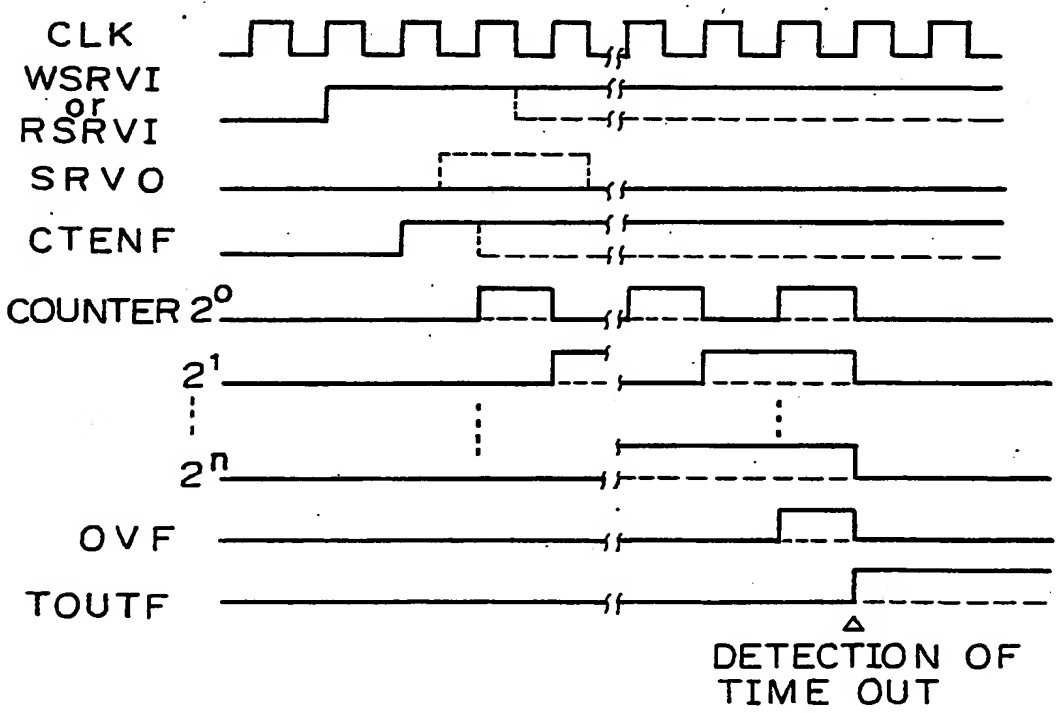
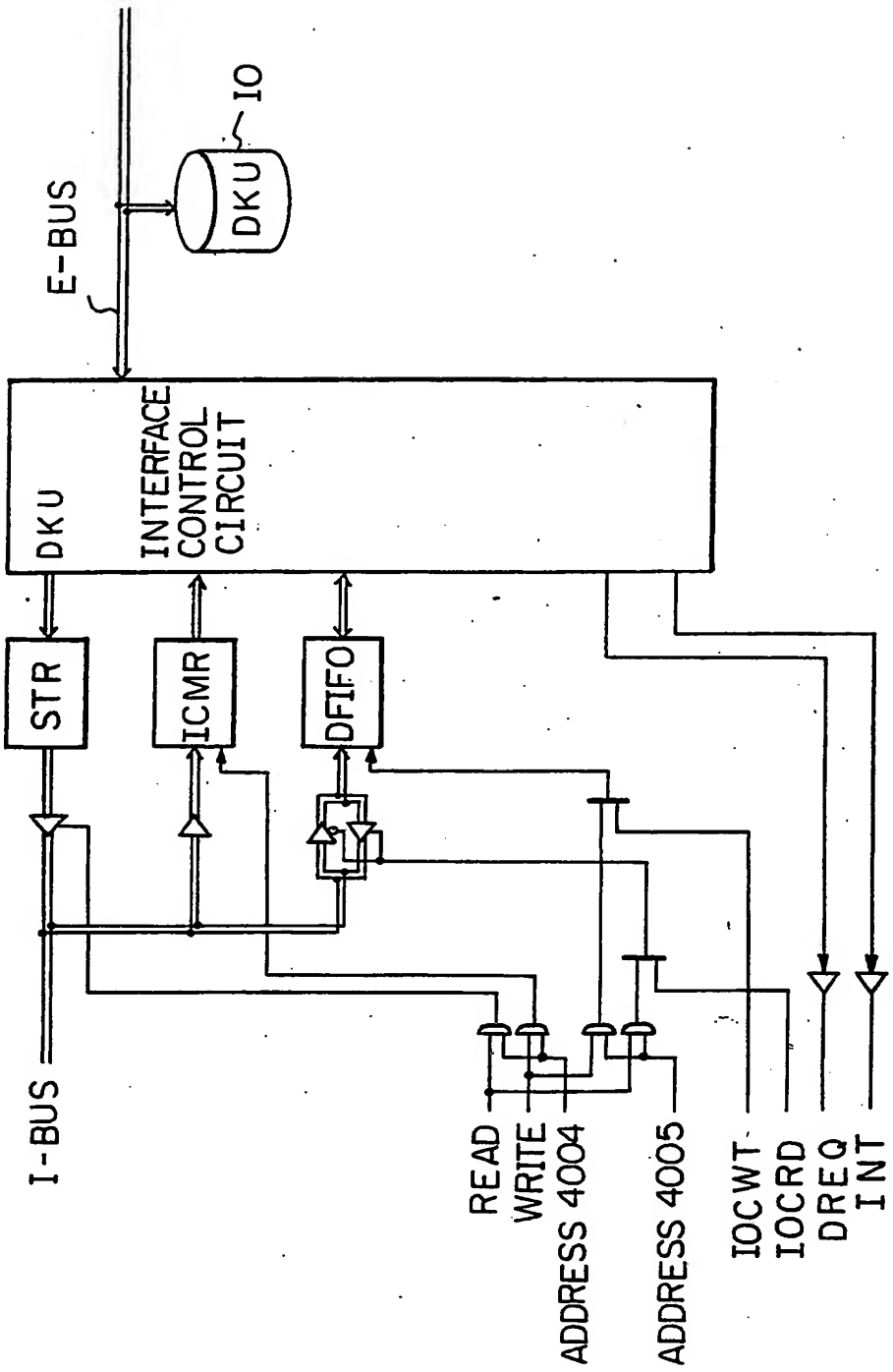

CLK
WSRVI
or
RSRVI
SRVO
CTENF
COUNTER 2^0
2^1
2^n
OVF
TOUTF
DETECTION OF
TIME OUT

Fig. 26


IOCTL
E-BUS
IO
DKU
DKU
INTERFACE CONTROL CIRCUIT
STR
ICMR
DFIFO
I-BUS
READ
WRITE
ADDRESS 4004
ADDRESS 4005
IOCWT
IOCRD
DREQ
INT